CLAIMS

We Claim:

1. A circuit for a memory module address bus comprising:

a transmission line comprising a dampening impedance between a driver and a branch point of said transmission line; and

a termination impedance having one end coupled to said transmission line between said dampening impedance and said branch point;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

2. The circuit of Claim 1, wherein said transmission line is uni-directional.

3. The circuit of Claim 1, wherein said ones of said branches are coupled to two memory module interfaces.

4. The circuit of Claim 1, wherein said ones of said branches are coupled to three memory module interfaces.

5. The circuit of Claim 1, wherein said ones of said branches are coupled to four memory module interfaces.

6. The circuit of Claim 1, wherein the distance from said branch point to said one end of said termination impedance is greater than the length of said branches.

7. The circuit of Claim 1, wherein said one end of said termination impedance is connected to said dampening impedance.

8. A circuit for reducing skew when addressing a memory module comprising:

a plurality of memory modules;

an address line coupling said memory modules;

a transmission line having a series impedance and a parallel impedance in a stub configuration; and

said transmission line having a first end coupled to a driver and a second end connected at a point on said address line to reduce skew when addressing a memory module.

9. The circuit of Claim 8, wherein said second end of said transmission line is connected at substantially the midpoint of said address line.

10. The circuit of Claim 8, wherein said transmission line is uni-directional.

11. The circuit of Claim 8, wherein said parallel impedance is connected to said series impedance.

12. The circuit of Claim 8, wherein said plurality of memory modules is an odd number and wherein said second end of said transmission line is connected to said address line at the middle memory module.

13. The circuit of Claim 8, wherein said plurality of memory modules is an even number and wherein said second end of said transmission line is connected to said address line at a point substantially midway between two memory modules closest to the mid-point of said address line.

14. A system for addressing memory modules comprising:

a bus controller;

a transmission line comprising a series impedance between a driver and a branch point of said transmission line; and

a parallel impedance having a first end coupled to said transmission line between said dampening impedance and said branch point and a second end coupled to a termination voltage terminal;

said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

15. The system of Claim 14, wherein two branches of said branches from said branch point have substantially the same length.

16. The system of Claim 14, wherein said transmission line is uni-directional.

17. The circuit of Claim 14, wherein said ones of said branches are coupled to two memory module interfaces.

18. The system of Claim 14, wherein said ones of said branches are coupled to three memory module interfaces.

19. The system of Claim 14, wherein said ones of said branches are coupled to four memory module interfaces.

20. The system of Claim 14, wherein the distance from said branch point to said first end of said parallel impedance is greater than the length of said branches.

21. The system of Claim 14, wherein said first end of said parallel impedance is connected to said series impedance.

22. The system of Claim 14, wherein said parallel impedance and said series resistance are mounted on opposite sides of a printed circuit board.